

FIG.1A

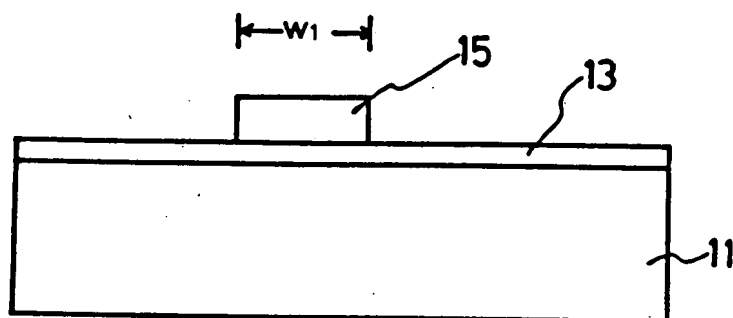


FIG.1B

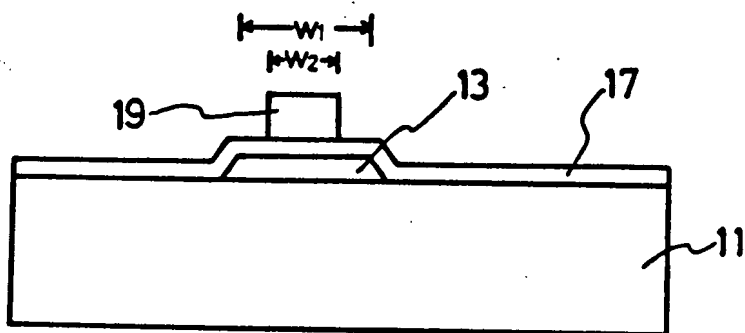
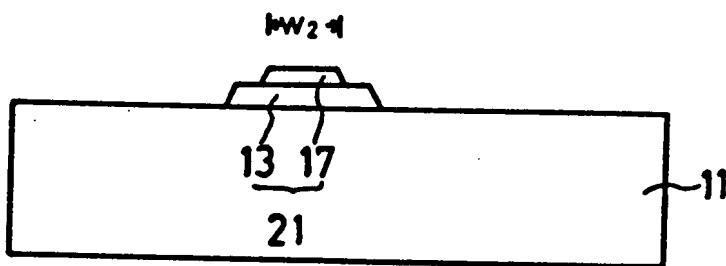


FIG.1C



14 FIG. 1C

FIG.1D

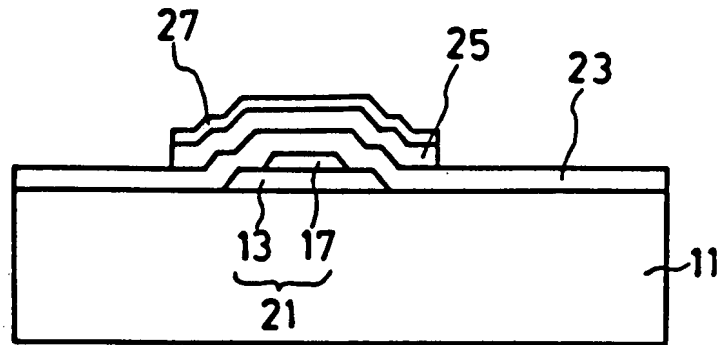


FIG.1E

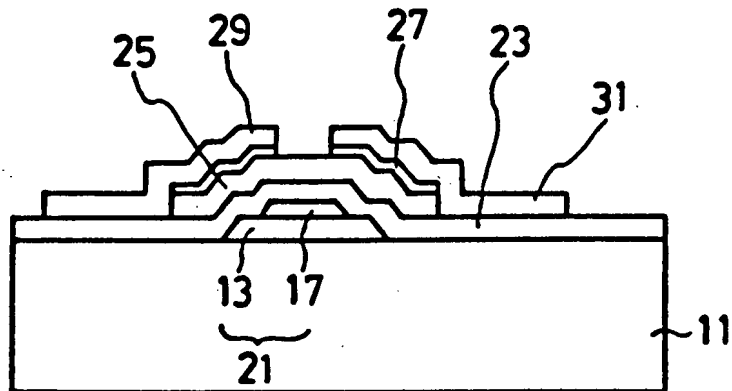


FIG.1F

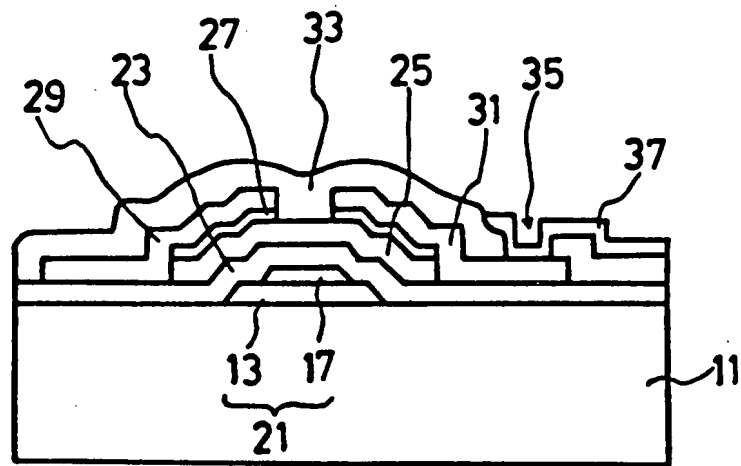


FIG.2

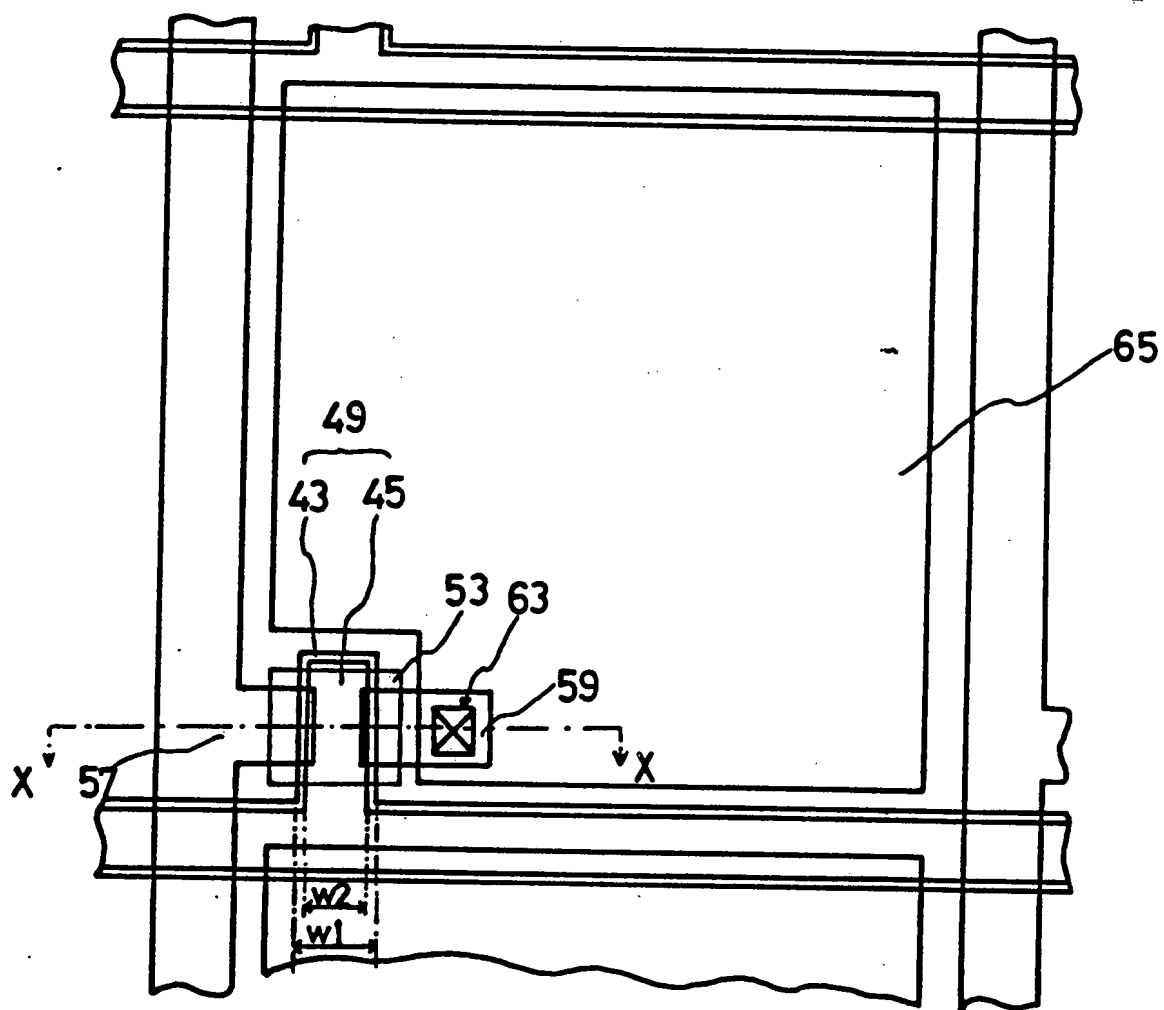


FIG.3

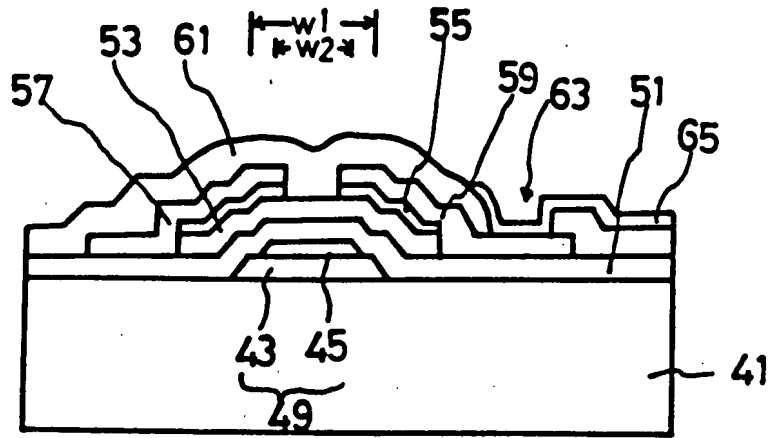


FIG.4A

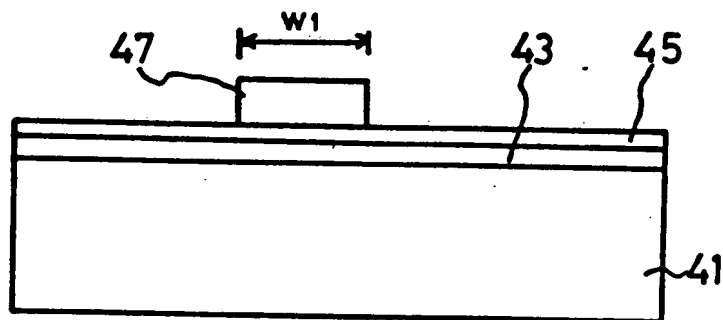


FIG.4B

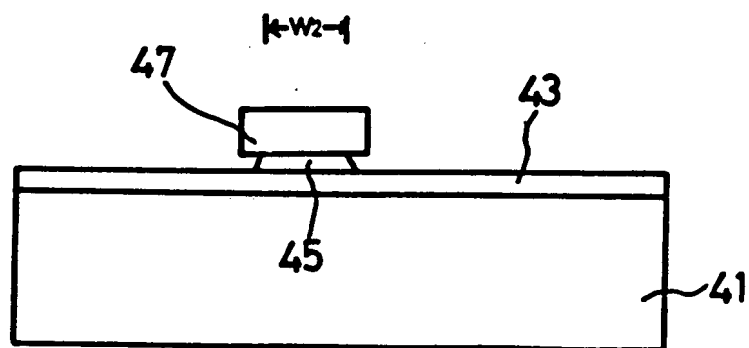


FIG.4C

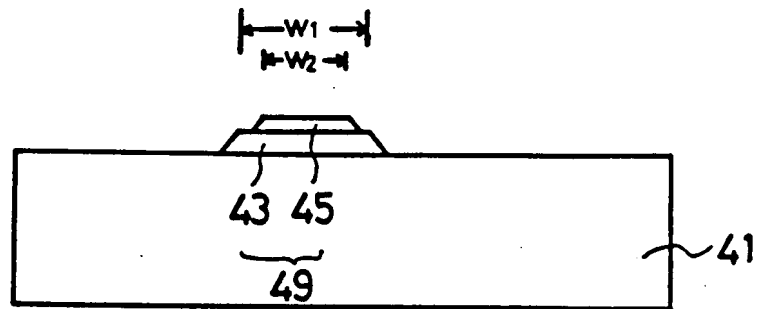


FIG.4D

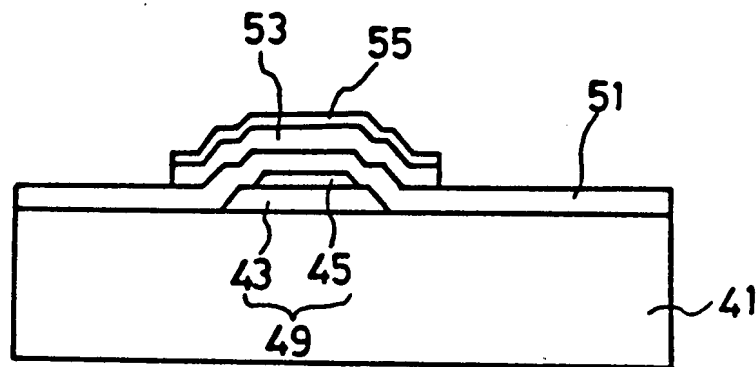


FIG.4E

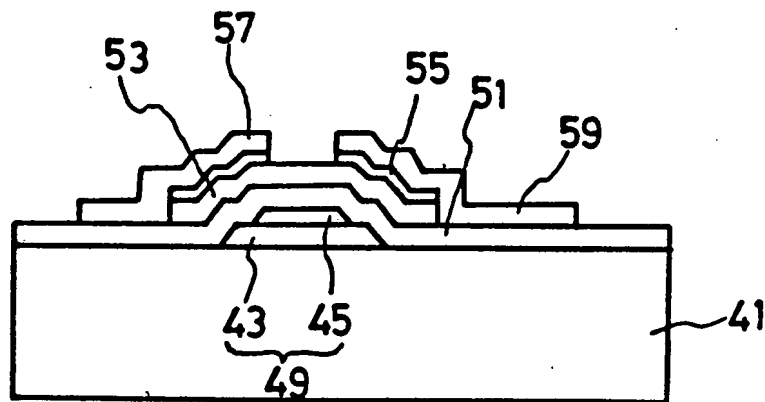


FIG. 4F

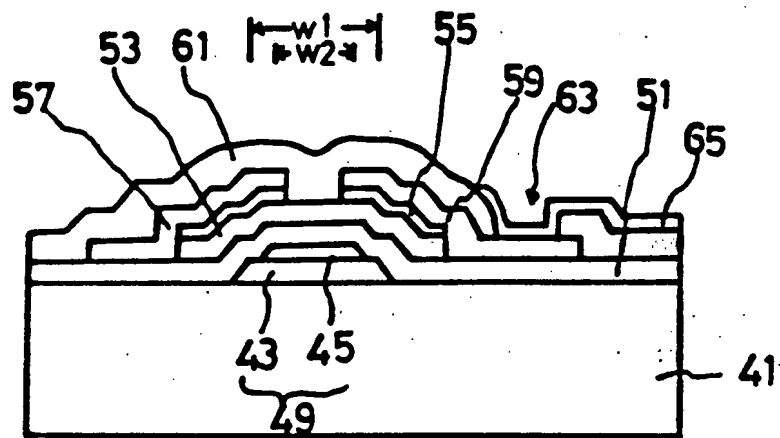


FIG.1A

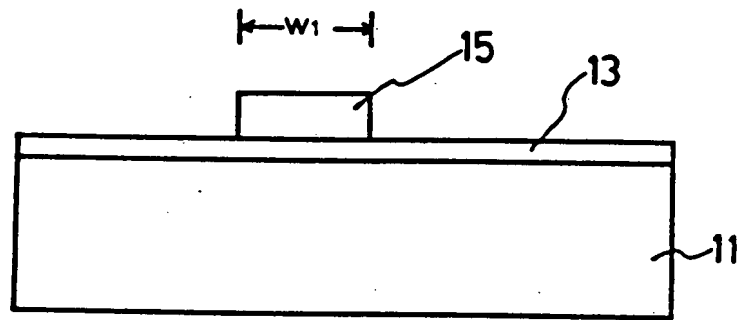


FIG.1B

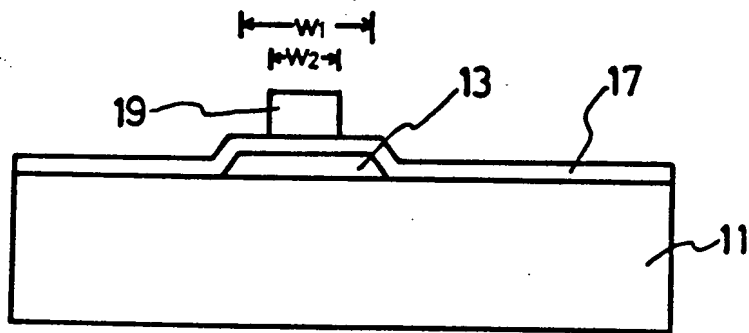
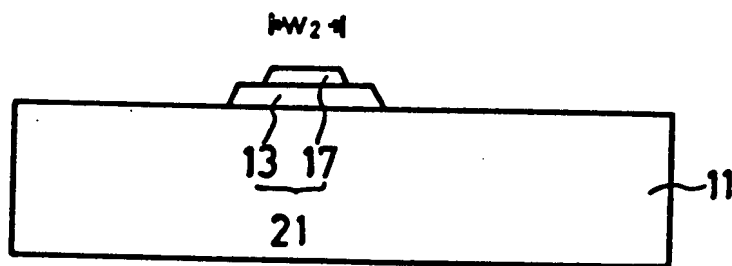
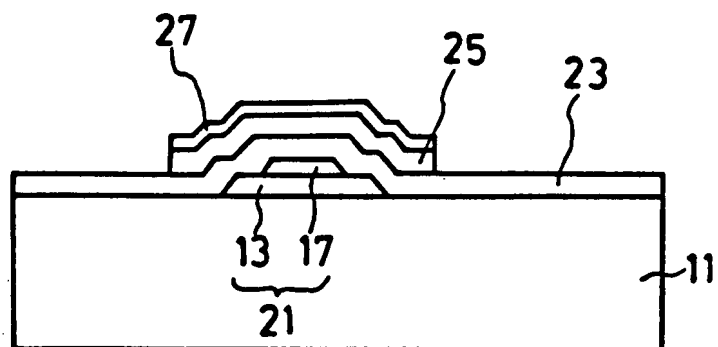
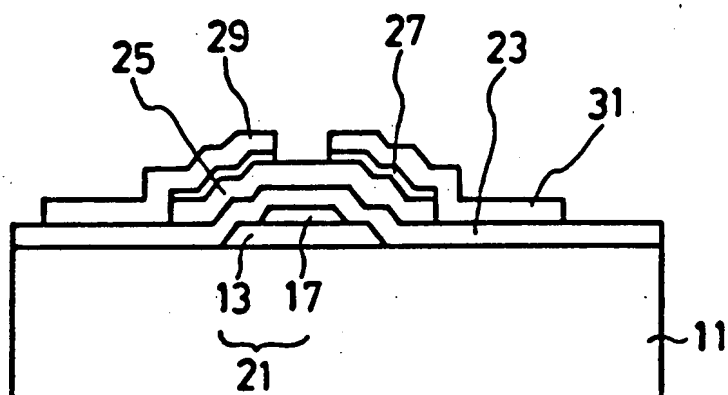


FIG.1C





A cross-sectional view of a semiconductor device. A substrate 11 is shown at the bottom. On top of the substrate, there is a layer 21 which contains two sub-layers, 13 and 17. Above layer 21, there is a series of stacked, stepped layers. From left to right, these layers are labeled 25, 29, 27, 23, and 31. The layers are connected by vertical vias or contacts.



A cross-sectional view of a semiconductor device. The device consists of a substrate 11 with a thin layer 21 on top. Layer 21 is composed of two sub-layers, 13 and 17. Above layer 21 is a series of stacked, wavy layers. From bottom to top, these layers are labeled 23, 25, 27, 29, 31, 33, 35, and 37. The top surface of the device is highly irregular and wavy.

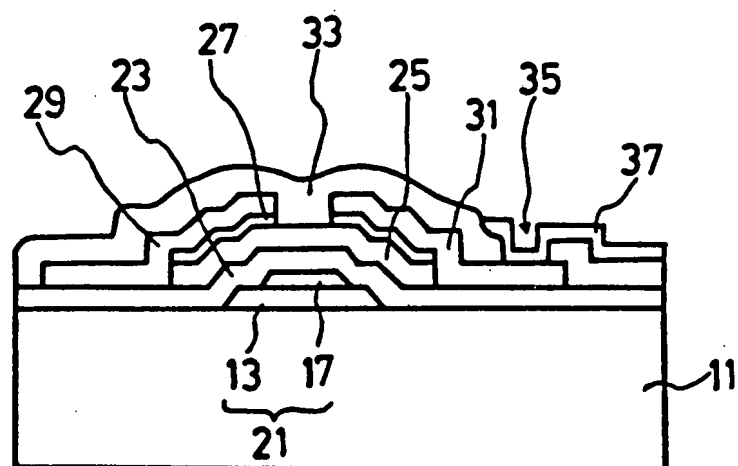
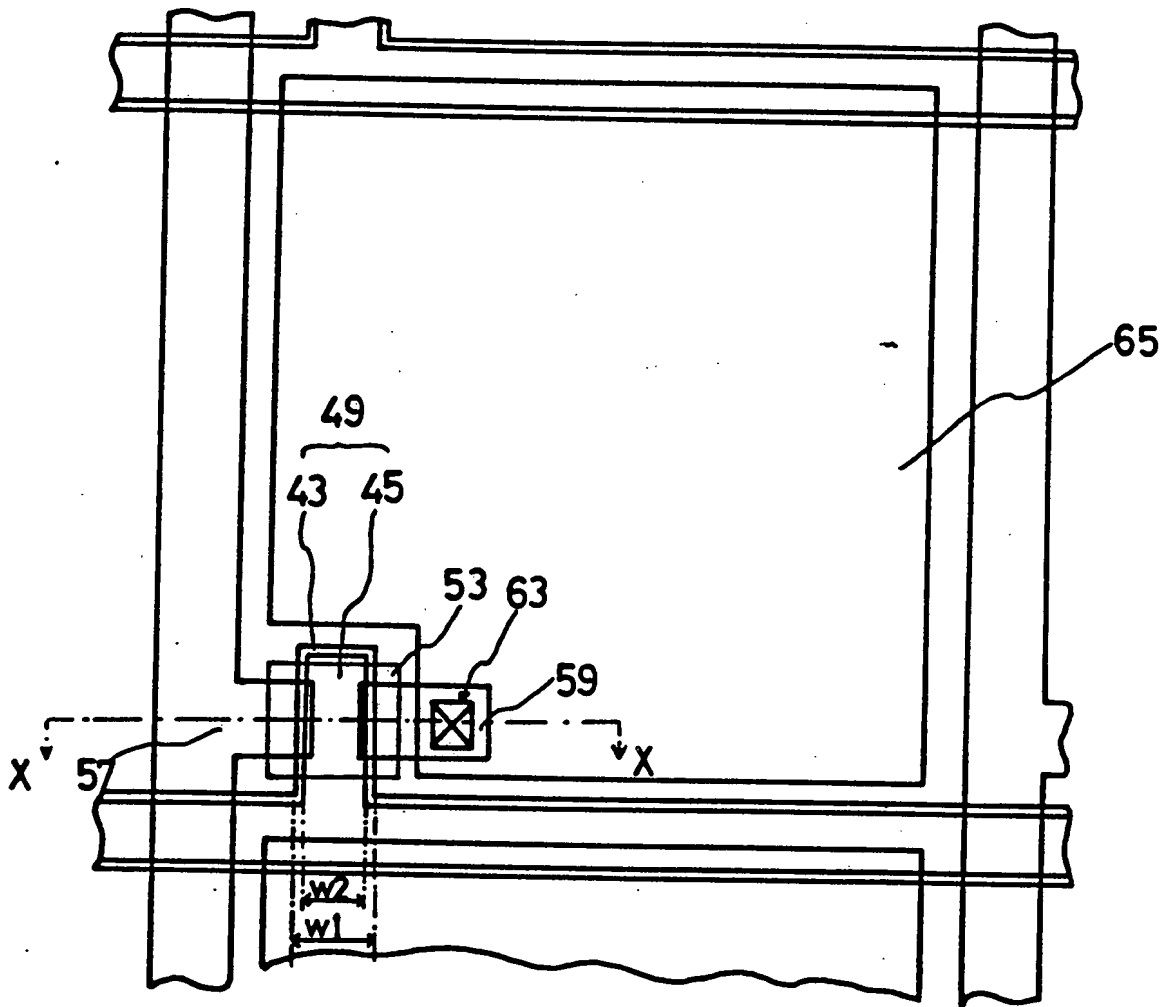


FIG.2



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262280* 5T18T680

FIG.3

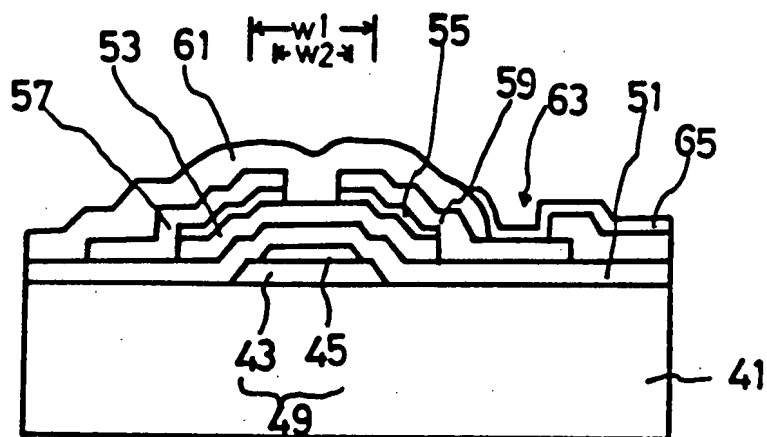


FIG.4A

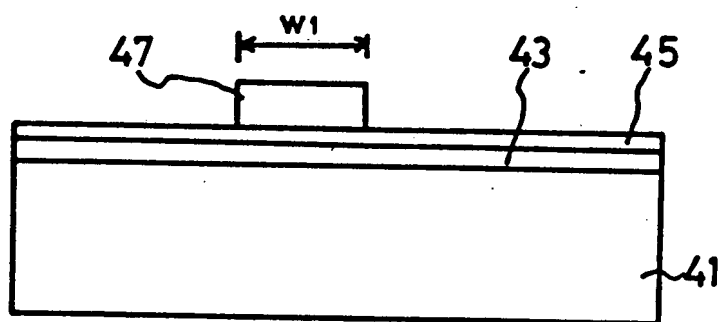


FIG.4B

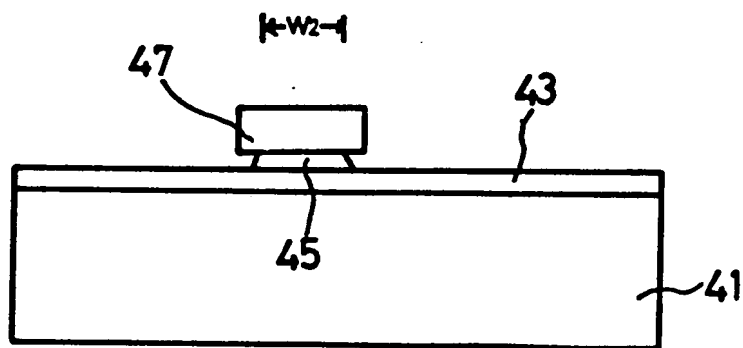


FIG.4C

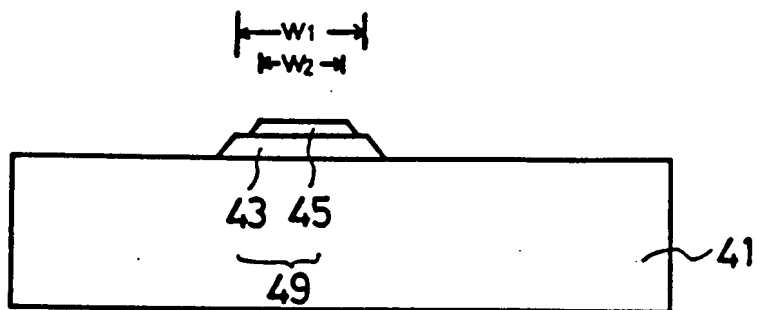


FIG.4D

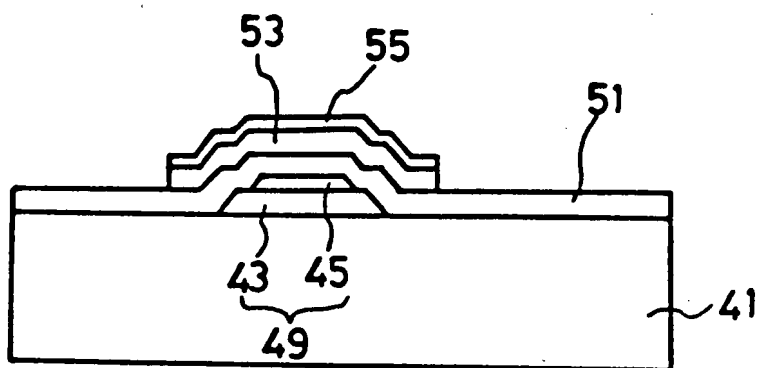
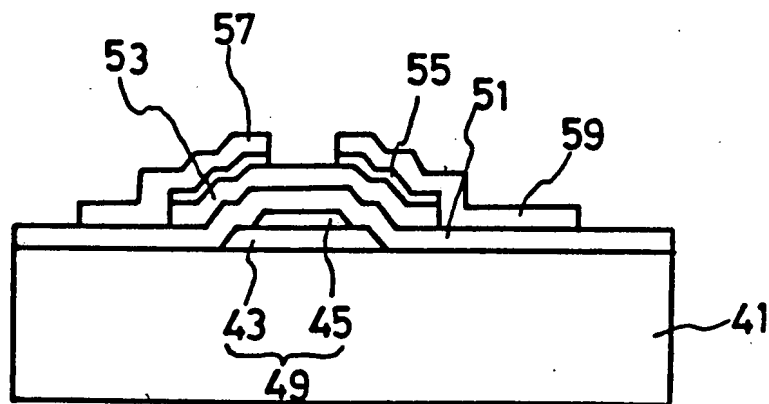


FIG.4E



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FIG.4F

